Amplifier Array for 12 Parallel 10 Gb/s Optical-Fiber Links Fabricated in a SiGe Production Technology

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Abstract — **A transimpedance amplifier array for 12 parallel optical-fiber channels each operating at 10 Gb/s is presented. It stands out for the following features: high gain (transimpedance 25 kΩ in the limiting mode), high input sensitivity and wide input dynamic range (input current swing from 20 to 240 μA_{p-p}), constant output voltage swing (differential 0.5 V_{p-p} at 50 Ω load) and low power consumption (1.4 W) at a single supply voltage (5V). Each channel has its own offset current control circuit. To the best of the authors' knowledge, the total throughput of 12 x 10 Gb/s = 120 Gb/s is the highest value reported for a single-chip amplifier array.**

I. Introduction

The dramatically increasing demands for high bandwidth in advanced electronic systems (like multiprocessor units and terabit/s-class switching systems) require high-speed interconnections [1], [2]. For short distances (up to several 100 m) parallel optical-fiber links are one of the favored solutions. Transmitter and receiver modules with 12 channels and data rates up to 2.7 Gb/s per channel have just been put on the market [3]. For example, Infineon Technologies offers a system called PAROLI: A linear 12 VCSEL array is driven by a Si transmitter chip and at the end of the 12 parallel multimode fibers a linear photodiode array drives a Si receiver chip consisting of 12 high-gain transimpedance amplifier channels [2].

Now the question arises: Can the data rate per fiber be further increased, e.g. up to 10 Gb/s ? From several announcements and publications it is expected that 10 Gb/s VCSEL arrays will be available in near future. However, to the best of the authors' knowledge it has not yet been demonstrated that the most critical electronic component in a 12-channel link, i.e. the array of 10 Gb/s high-gain transimpedance amplifiers, can be integrated on a single chip at low costs and low power consumption, without running into crosstalk problems between the channels. In order to contribute to this question, such an amplifier array was developed and fabricated in a SiGe bipolar production technology. The target specifications, some of which agree with the most recent PAROLI system [4], are:

- Range of input current swing: ΔI_I = 20 to 240 μA_{p-p}.
- On-chip automatic offset control to compensate for the average input current (half of ΔI_I).
- Differential outputs with constant swing: ΔV_Q = 0.5 V_{p-p} at 50 Ω external load (terminated transmission lines). In addition, 100 Ω output resistors are provided on the chip to reduce double reflections.
- Single supply voltage: +5 V or –5 V, as an option (different circuit versions).
- Power consumption: 1.4 W. It can be reduced by 12 % if the output swing is reduced to 0.3 V_{p-p} via a single bond pad (option).
- On-chip generation of the bias voltage for the (pin) photodiodes.

II. Circuit Principle And Design Aspects

Before we go into details, a layout of the amplifier array is given in Fig. 1, with its 12 differential inputs and outputs. It is drawn by superposing the four metallization layers of the final layout.

First, a single amplifier channel (row) will be discussed. The simplified block diagram is shown in Fig. 2. The circuit is driven by the photodiode (PD) and loaded by terminated 50 Ω transmission lines. It consists of 3 similar amplifier cells. The circuit diagram of the first cell is given in Fig. 3. The circuit principle used and the design aspects are very similar to the 40 Gb/s transimpedance amplifier described in [5]-[7], so that we can restrict ourselves to few remarks. The output voltage swing ΔV_Q is kept constant (differential 2 x 0.25 V = 0.5 V_{p-p}) by operating at least the last stage in the limiting mode. This condition must be met even for the minimum input current swing (ΔI_I = 20 μA_{p-p}), resulting in a maximum (nonlinear) transimpedance as high as 25 kΩ. Important aspects for the design of a single amplifier row are ([5] - [10]):

- The principle of strong impedance mismatching between succeeding stages allows high constant gain from dc up to high frequencies. Here, an amplifier cell (see Fig. 3) starts with a transimpedance stage (TIS) suc-

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ceeded by an emitter follower pair (EF) and a transadmittance stage (TAS), which drives the comparatively long microstrip-line to the next cell (in the next column).

- The group delay of the first linear operating stages has to be as constant as possible up to about 7.5 GHz in order to reduce time jitter, while a 3 dB cutoff frequency of only 5 GHz can be tolerated due to the amplitude limitation by the output stage [5] - [7].

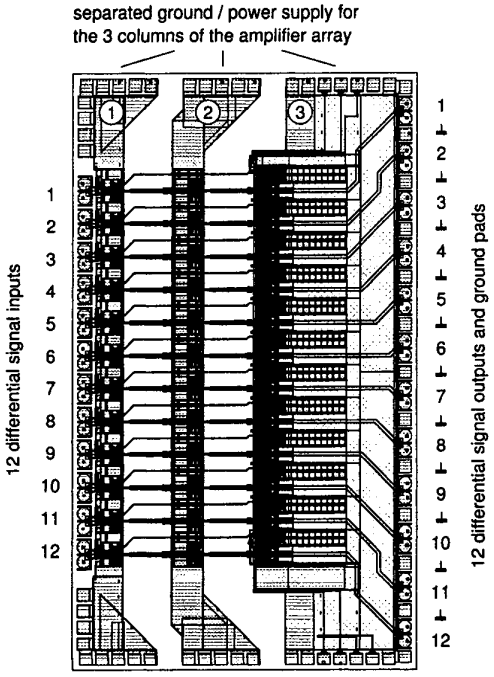

Fig. 1. Layout of the amplifier array with 12 differential inputs and outputs showing 3 columns with separate ground and power supply. A row consists of 3 amplifier cells connected by differential microstrip lines. The chip size is 2.8 mm x 4.6 mm.

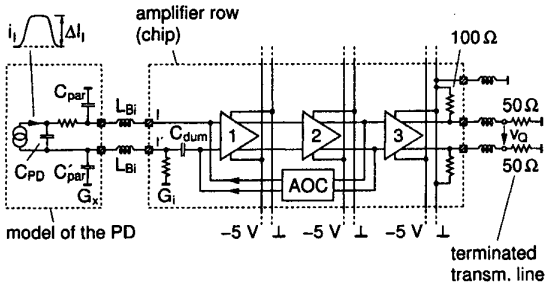

Fig. 2. Simplified block diagram of the limiting transimpedance amplifier in a row of the array, consisting of 3 amplifier cells and an automatic offset-current control (AOC) circuit.

Moreover, the driving and loading conditions (incl. the bond inductances) are shown.

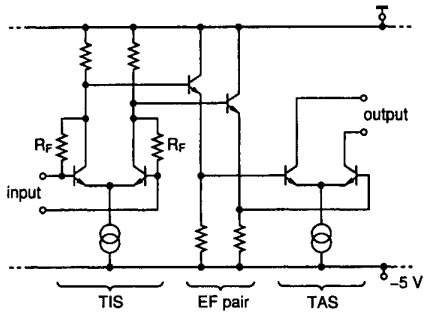

Fig. 3. Simplified circuit diagram of the first amplifier cell in Fig. 2. Apart from the currents and transistor dimensions, the 3 cells in a row differ only slightly: The second and third cell use an EF pair in the feedback path of the TIS and an additional EF pair in front of the TAS. In the third cell two on-chip 100 Ω output resistors are provided.

- The high input sensitivity (low minimum input current swing) requires a low equivalent input noise current (here about 1 μA_{rms}). For this, the transimpedance (R_F) of the first amplifier stage is chosen as high as possible.
- The differential input pads are directly bonded to the two bond pads of the PD. In series to the complementary input I' an on-chip capacitor C_{dum} is used which acts as a dummy for the PD capacitance C_{PD} (here 0.15-0.2 pF). This measure eliminates the need for a decoupling (off- or on-chip) capacitor with its inherent problems and makes the amplifier less sensitive to noise on the on-chip ground G_i (mainly generated by the other 11 channels).
- Due to the high number of amplifier channels, the power consumption per channel has to be kept as low as possible. Including the offset current control, only 23.3 mA per channel are required, resulting in a total power of 1.4 W. It can be further reduced (as an option) by reducing the output voltage swing (to 0.3 V_{p-p}).

A dc current of half the input current swing ΔI_I has to be fed into the input of each amplifier to compensate for the dc part of the input signal. It is generated by an automatic offset control (AOC) circuit (see Fig. 2) which shall not be discussed here. Together with the large MOS capacitors required (100 pF per channel) the 12 AOCs are located on the right-hand side of the third column in Fig. 1.

As the most challenging and time consuming part of the design, the crosstalk between the channels had to be investigated and minimized. This is a severe problem of such an array due to the high bandwidth and high gain of the amplifiers as well as to the small channel pitch (250 µm) and the long on-chip supply lines (see Fig. 1). Numerous careful simulations with special regard to the

influence of distributed on-chip metallization, of mounting parasitics (especially bond inductances), and of the substrate (using our simulator SUSI [11]) were required, in order to find out adequate measures to drop the interaction between the channels to a sufficiently low level.

Several measures for crosstalk reduction used by us in earlier designs (but restricted to a single amplifier channel) were also applied here ([5] - [9]):

- Differential circuit configuration.
- Separate ground and power supply, respectively, for the different amplifier cells (cf. Fig. 1).
- Comparatively long distances between the cells (see rows in Fig. 1), with the channel stopper eliminated between them to increase the lateral substrate impedance.
- Guard rings around each cell.
- Decoupling capacitors between on-chip power supply and ground at each amplifier cell, realized by MIM capacitors and by the capacitances between the 4 metallization layers.
- Common shield for each pair of input pads.
- Decoupling resistors in the (long) offset-current line.

However, crosstalk is much more critical in an amplifier *array* compared to a single channel since the noise contribution of the other 11 channels can build up a high noise amplitude. This especially holds if - under worst-case conditions - all output cells switch simultaneously. Moreover, as obvious from Fig. 1, the cells in the middle of the first and second row need long ground and supply lines and suffer, therefore, under comparatively large parasitic inductances (in addition to the bond inductances). As a consequence, the ground nodes of these cells are quite noisy, especially due to the common-mode current noise generated by the circuit. Therefore, the following additional measures were taken to reduce crosstalk:

- A large ground plate between the third column of amplifier cells (output stages) and the right-hand edge of the chip (see Fig. 1) is used, which is connected via numerous bonds to the external ground.
- Coupling of the chip-substrate to the (low-noise) ground of the module is made as strong as possible, e.g. by reducing the glue thickness if the chip is mounted on the socket by an insulating glue.
- At the inputs I', on-chip dummy capacitors (C_{dum}) are provided, as mentioned before. Thus the noise at the critical internal ground node G_i is split up and fed into *both* inputs. If the influences of the parasitic capacitances C_{par} , C'_{par} and bond inductances L_{Bi} (see Fig. 2) were negligible, noise compensation would be perfect.

III. Realization And Experimental Results

The chip was fabricated in the SiGe bipolar production technology B7HF of Infineon Technologies [12]. It is a self-aligned double-poly-silicon technology with 4 metallization layers. A Ge gradient in the epitaxial base increases f_T and thus f_{max} to values between 70 and 75 GHz. Vertical pnp transistors, as well as MIS and MIM capacitors are available and were used in this circuit. For measurements, the chip was mounted on a self-made measurement socket as described in [7], [8], using conventional wire bonding. Since the VCSEL and PD arrays were not available at the beginning, the PD was modeled by an electrical RC network which was driven by a pseudo-random pulse generator (word length 2^{23} - 1 bit) [6].

Fig. 4a shows the measured output eye diagrams of a single channel (No. 7, cf. Fig. 1) at 10 Gb/s for the interesting range of input current swing ΔI_I (20 to 240 μA_{p-p}). In all cases, a clear eye diagram at constant output swing of 500 mV_{p-p} (differential) is obtained. Even at a further reduced input signal, ΔI_I = 15 μA_{p-p} , the measured bit error rate (BER) is still as low as 10^{-11}. It should be mentioned that, due to the limited resistance used to approximate the PD current source (i_I in Fig. 2), the input sensitivity measured in this way is worse compared to the value expected if the circuit is driven by a real PD (current source). Simulations let us expect a difference of about 30 %.

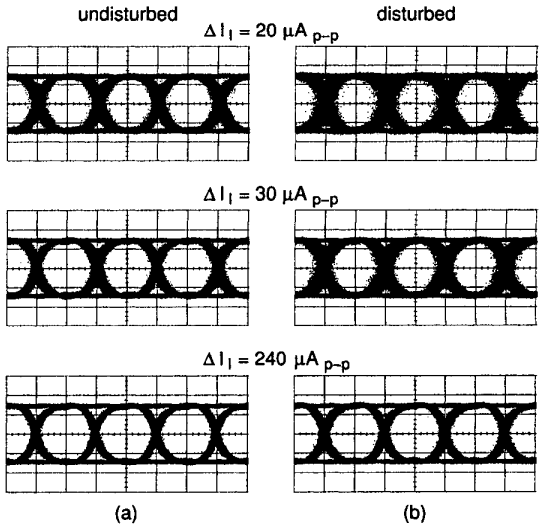

Fig. 4. Measured output eye diagrams (v_O) of an amplifier channel (No. 7) at 10 Gb/s for different input current swings ΔI_I. (a) undisturbed. (b) disturbed by the other 11 channels. In all cases, the output voltage swing is 500 mV_{p-p}. Vertical: 160 mV/div., horizontal: 50 ps/div.

To analyze crosstalk, two disturbing amplifier blocks were built with the disturbed amplifier channel under test (No. 7 in Fig. 1) located between them. The first block consists of the channels 1 to 6 and the second one of the channels 8 to 12. The amplifier inputs within a block are connected. The input pulse sequence which drives block 2 is delayed by several bit widths with respect to the input sequence of block 1 and to the amplifier channel under test. All the 12 channels have the same input current swing. It should be pointed out that the conditions of these (purely electrical) measurements and thus the results presented below are too pessimistic compared to the intended practical application for the following reasons:

- All channels within a disturbing amplifier block are driven by the same pulse sequence and are switched simultaneously, so that the generated noise peaks are added.
- The parasitic capacitances C_{par} , C'_{par} of the electrical PD model (cf. Fig. 2) can not be made as low as in the case of a real PD. This fact considerably increases the crosstalk caused by the noisy internal ground G_i, as confirmed by simulations (cf. Section II).
- The two stubs on the measuring socket which provide all disturbing channels with input signals are comparatively long. Their parasitic inductances increase crosstalk, as again shown by simulating the influence of the measuring socket on circuit performance.

Fig. 4b shows the output eye diagrams of the channel under test if disturbed by the other 11 channels under the (too pessimistic) crosstalk conditions described above. At low input current swings, the jitter is now substantially increased due to the crosstalk. However, the measured BER is still around 10^{-10} at the minimum ΔI_I of 20 $\mu A_{p\text{-}p}$, while at $\Delta I_I = 30\ \mu A_{p\text{-}p}$ no errors were detected within 4 minutes (BER < 10^{-12}). It is worth while to note that the jitter of the eye diagram is drastically reduced and approximates that in Fig. 4a (undisturbed case) if the channel under test is only disturbed by a single block (6 disturbing channels). Now at minimum ΔI_I (20 $\mu A_{p\text{-}p}$) no errors were detected within 4 minutes (BER < 10^{-12}). All these results let us expect that the transimpedance amplifier array is well suited for the intended application.

Shortly before the deadline of the final manuscript, first optical measurements of a single amplifier channel have been performed. They confirm the good results obtained for an electrically driven amplifier array. Further results will be presented at the conference.

IV. Conclusions

A transimpedance amplifier array for 12 parallel optical-fiber links each operating at 10 Gb/s is presented. To the best of the authors' knowledge the total throughput of 120 Gb/s is the highest value reported for such an integrated circuit. Crosstalk problems between the high-gain channels with only 250 µm pitch on the chip have been solved by careful design considerations and simulations. The use of a high-yield SiGe production technology and of a conservative mounting technique as well as the low power consumption of 1.4 W reduce the costs of the receiver module. The 12 output buffer stages of the circuit are well suited to drive the succeeding clock and data recovery array directly.

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